

General-purpose single bipolar timers

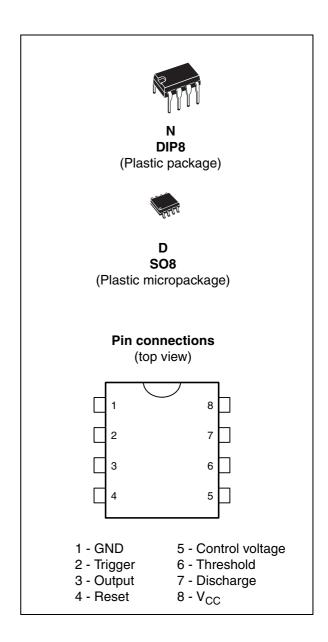
Features

- Low turn-off time
- Maximum operating frequency greater than 500 kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- Output can source or sink up to 200 mA
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

Description

The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor.

The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA.



1 Schematic diagrams

Figure 1. Block diagram

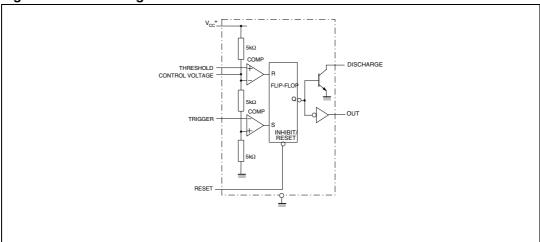
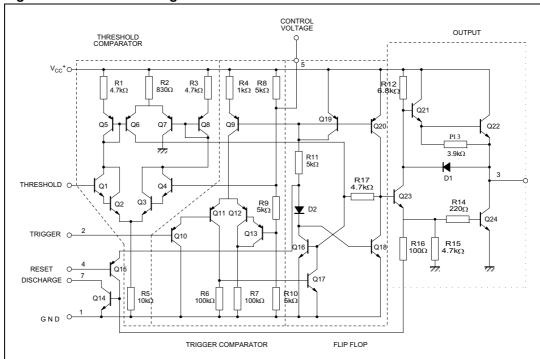


Figure 2. Schematic diagram



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage	18	V
I _{OUT}	Output current (sink & source)	±225	mA
R _{thja}	Thermal resistance junction to ambient ⁽¹⁾ DIP8 SO-8	85 125	°C/W
R _{thjc}	Thermal resistance junction to case ⁽¹⁾ DIP8 SO-8	41 40	°C/W
	Human body model (HBM) ⁽²⁾	1000	
ESD	Machine model (MM) ⁽³⁾	100	V
	Charged device model (CDM) ⁽⁴⁾	1500	
	Latch-up immunity	200	mA
T _{LEAD}	Lead temperature (soldering 10 seconds)	260	°C
Tj	Junction temperature	150	°C
T _{stg}	Storage temperature range	-65 to 150	°C

- 1. Short-circuits can cause excessive heating. These values are typical.
- 2. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a $1.5 \mathrm{k}\Omega$ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
- 3. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
- 4. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage NE555 SA555 SE555	4.5 to 16 4.5 to 16 4.5 to 18	٧
$V_{th}, V_{trig}, \ V_{cl}, V_{reset}$	Maximum input voltage	V_{CC}	>
l _{OUT}	Output current (sink and source)	±200	mA
T _{oper}	Operating free air temperature range NE555 SA555 SE555	0 to 70 -40 to 105 -55 to 125	°C

3 Electrical characteristics

Table 3. T_{amb} = +25° C, V_{CC} = +5 V to +15 V (unless otherwise specified)

Cumbal	Parameter	SE555			NE555 - SA555			Unit
Symbol	Falametei		Тур.	Max.	Min.	Тур.	Max.	Unit
I _{CC}	Supply current (R _L = ∞) Low state V_{CC} = +5V V_{CC} = +15V High state V_{CC} = +5V		3 10 2	5 12		3 10 2	6 15	mA
	Timing error (monostable) $(R_A = 2k\Omega to 100k\Omega C = 0.1\mu F)$ Initial accuracy $^{(1)}$ Drift with temperature Drift with supply voltage		0.5 30 0.05	2 100 0.2		1 50 0.1	3 0.5	% ppm/°C %/V
	Timing error (astable) ($R_{A,}R_{B}=1k\Omega$ to 100kΩ C = 0.1μF, $V_{CC}=+15V$) Initial accuracy ⁽¹⁾ Drift with temperature Drift with supply voltage		1.5 90 0.15			2.25 150 0.3		% ppm/°C %/V
V _{CL}	Control voltage level V _{CC} = +15V V _{CC} = +5V	9.6 2.9	10 3.33	10.4 3.8	9 2.6	10 3.33	11 4	V
V _{th}	Threshold voltage V _{CC} = +15V V _{CC} = +5V	9.4 2.7	10 3.33	10.6 4	8.8 2.4	10 3.33	11.2 4.2	V
I _{th}	Threshold current (2)		0.1	0.25		0.1	0.25	μΑ
V _{trig}	Trigger voltage $V_{CC} = +15V$ $V_{CC} = +5V$	4.8 1.45	5 1.67	5.2 1.9	4.5 1.1	5 1.67	5.6 2.2	V
I _{trig}	Trigger current (V _{trig} = 0V)		0.5	0.9		0.5	2.0	μA
V _{reset}	Reset voltage (3)	0.4	0.7	1	0.4	0.7	1	V
I _{reset}	Reset current V _{reset} = +0.4V V _{reset} = 0V		0.1 0.4	0.4 1		0.1 0.4	0.4 1.5	mA
V _{OL}	Low level output voltage $V_{CC} = +15V I_{O(sink)} = 10 \text{mA}$ $I_{O(sink)} = 50 \text{mA}$ $I_{O(sink)} = 100 \text{mA}$ $I_{O(sink)} = 200 \text{mA}$ $V_{CC} = +5V I_{O(sink)} = 8 \text{mA}$ $I_{O(sink)} = 5 \text{mA}$		0.1 0.4 2 2.5 0.1 0.05	0.15 0.5 2.2 0.25 0.2		0.1 0.4 2 2.5 0.3 0.25	0.25 0.75 2.5 0.4 0.35	V
V _{OH}	High level output voltage $V_{CC} = +15V I_{O(sink)} = 200 mA$ $I_{O(sink)} = 100 mA$ $V_{CC} = +5V I_{O(sink)} = 100 mA$	13 3	12.5 13.3 3.3		12.75 2.75	12.5 13.3 3.3		V

Table 3. T_{amb} = +25° C, V_{CC} = +5 V to +15 V (unless otherwise specified) (continued)

Symbol	Parameter	SE555			NE555 - SA555			Unit
	raiametei		Тур.	Max.	Min.	Тур.	Max.	5
I _{dis(off)}	Discharge pin leakage current (output high) $V_{dis} = 10V$		20	100		20	100	nA
V _{dis(sat)}	Discharge pin saturation voltage (output low) $^{(4)}$ $V_{CC} = +15V$, $I_{dis} = 15mA$ $V_{CC} = +5V$, $I_{dis} = 4.5mA$		180 80	480 200		180 80	480 200	mV
t _r	Output rise time Output fall time		100 100	200 200		100 100	300 300	ns
t _{off}	Turn off time $^{(5)}$ ($V_{reset} = V_{CC}$)		0.5			0.5		μs

- 1. Tested at V_{CC} = +5 V and V_{CC} = +15 V.
- 2. This will determine the maximum value of R_A + R_B for 15 V operation. The maximum total $(R_A + R_B)$ is 20 M Ω for +15 V operation and 3.5 M Ω for +5 V operation.
- 3. Specified with trigger input high.
- 4. No protection against excessive pin 7 current is necessary, providing the package dissipation rating is not exceeded.
- 5. Time measured from a positive pulse (from 0 V to 0.8 x V_{CC}) on the Threshold pin to the transition from high to low on the output pin. Trigger is tied to threshold.

Figure 3. Minimum pulse width required for Figure 4. Supply current versus supply triggering voltage

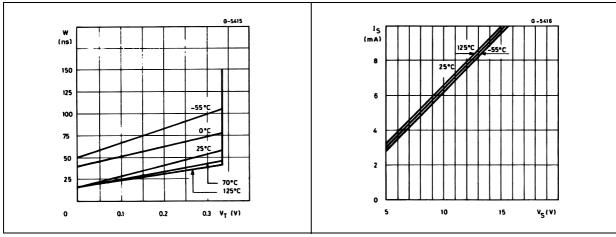


Figure 5. Delay time versus temperature

Figure 6. Low output voltage versus output sink current

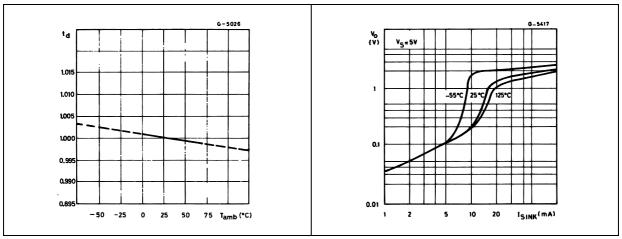


Figure 7. Low output voltage versus output sink current

Figure 8. Low output voltage versus output sink current

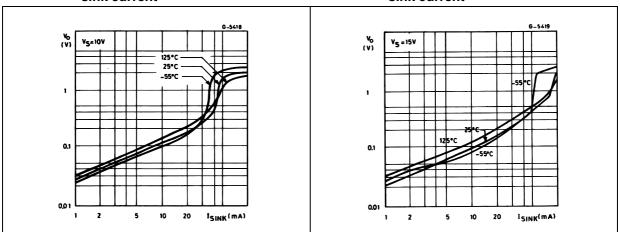


Figure 9. High output voltage drop versus output

Figure 10. Delay time versus supply voltage

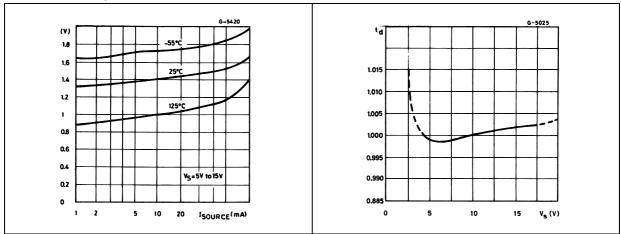
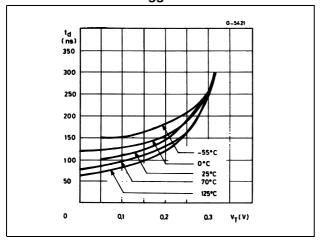


Figure 11. Propagation delay versus voltage level of trigger value



4 Application information

4.1 Monostable operation

In the monostable mode, the timer generates a single pulse. As shown in *Figure 12*, the external capacitor is initially held discharged by a transistor inside the timer.

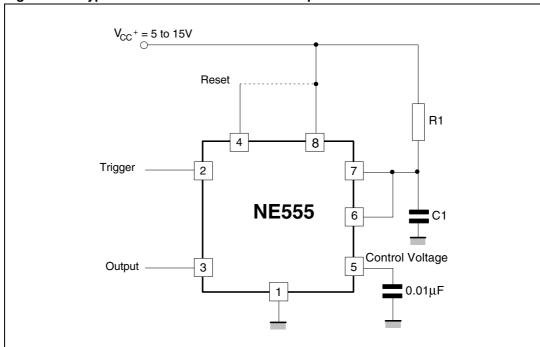


Figure 12. Typical schematics in monostable operation

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC} . Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1 R_1 C_1$ and is easily determined by *Figure 14*.

Note that because the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short-circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $t=R_1C_1$. When the voltage across the capacitor equals 2/3 V_{CC} , the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state.

Figure 13 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possibility of unwanted triggering.

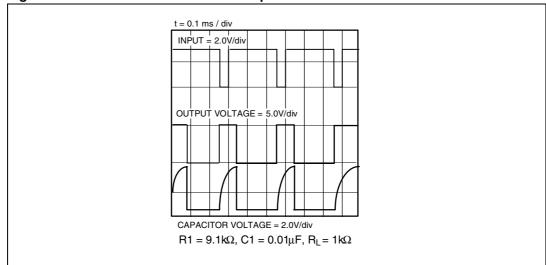
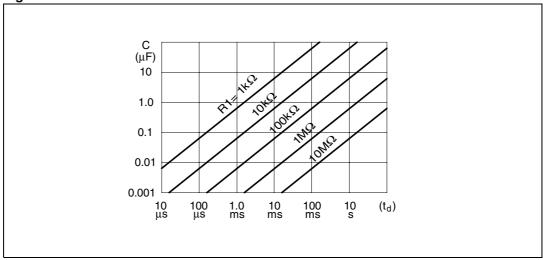


Figure 13. Waveforms in monostable operation

Figure 14. Pulse duration versus R1C1



4.2 Astable operation

When the circuit is connected as shown in *Figure 15* (pins 2 and 6 connected) it triggers itself and free runs as a multi-vibrator. The external capacitor charges through R_1 and R_2 and discharges through R_2 only. Thus the duty cycle can be set accurately by adjusting the ratio of these two resistors.

In the astable mode of operation, C_1 charges and discharges between 1/3 V_{CC} and 2/3 V_{CC} . As in the triggered mode, the charge and discharge times and, therefore, frequency are independent of the supply voltage.

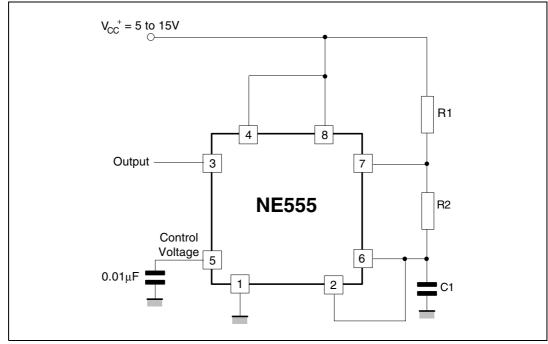


Figure 15. Typical schematics in astable operation

Figure 16 shows the actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t1 = 0.693 (R_1 + R_2) C_1$$

and the discharge time (output LOW) by:

$$t2 = 0.693 (R_2) C_1$$

Thus the total period T is given by:

$$T = t1 + t2 = 0.693 (R1 + 2R2) C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)C1}$$

It can easily be found from Figure 17.

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

Figure 16. Waveforms in astable operation

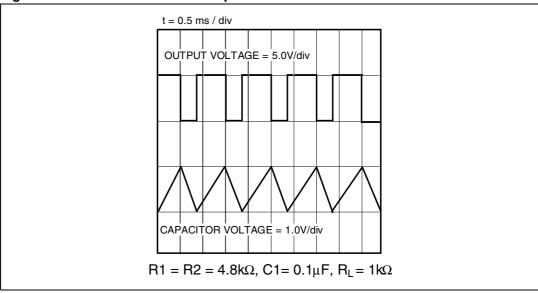
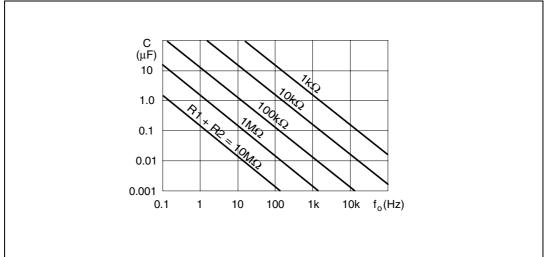


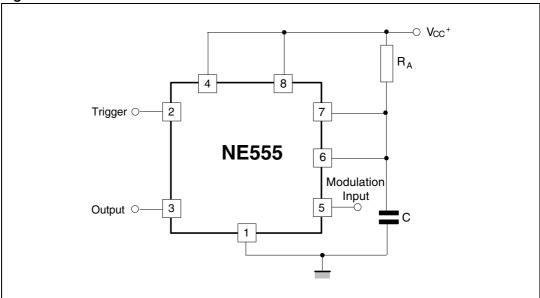
Figure 17. Free running frequency versus R₁, R₂ and C₁



4.3 Pulse width modulator

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 18* shows the circuit.

Figure 18. Pulse width modulator



4.4 Linear ramp

When the pull-up resistor, R_A , in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 19* shows a circuit configuration that will perform this function.

Figure 19. Linear ramp

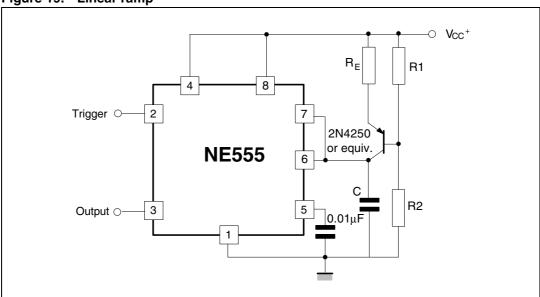
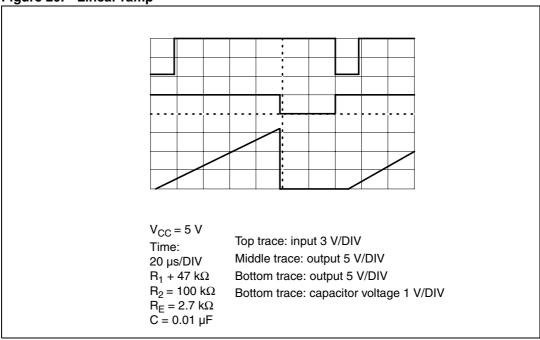


Figure 20 shows the waveforms generator by the linear ramp.

The time interval is given by:

$$T = \frac{(2/3 \text{ Vcc RE (R1+R2) C})}{\text{R1 Vcc - VBE (R1+R2)}} \text{ VBE} = 0.6 \text{V}$$

Figure 20. Linear ramp



4.5 50% duty cycle oscillator

For a 50% duty cycle, the resistors R_A and R_B can be connected as in *Figure 21*. The time period for the output high is the same as for a table operation (see *Section 4.2 on page 9*):

$$t1 = 0.693 R_A C$$

For the output low it is

$$t_2$$
= [(R. RB)/(RA+RB)].C.Ln $\left[\frac{RB-2RA}{2RB-RA}\right]$

Thus the frequency of oscillation is:

$$f = \frac{1}{t1 + t2}$$

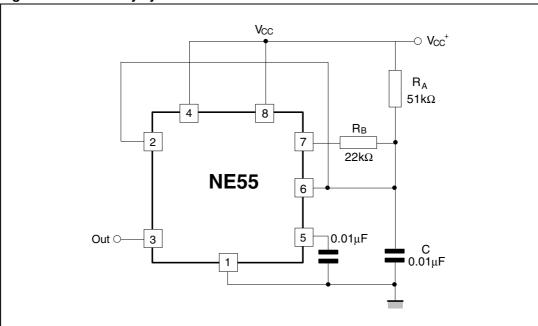


Figure 21. 50% duty cycle oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

4.6 Additional information

Adequate power supply bypassing is necessary to protect associated circuitry. The minimum recommended is 0.1 μ F in parallel with 1 μ F electrolytic.

5 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

5.1 DIP8 package information

Figure 22. DIP8 package mechanical drawing

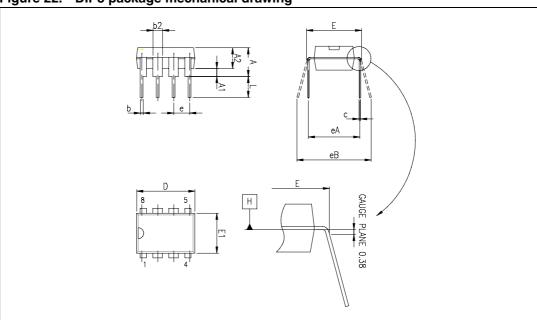


Table 4. DIP8 package mechanical data

			Dimer	nsions		
Ref.		Millimeters			Inches	
	Min.	Тур.	Max.	Min.	Тур.	Max.
Α			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
С	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
е		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

5.2 SO-8 package information

Figure 23. SO-8 package mechanical drawing

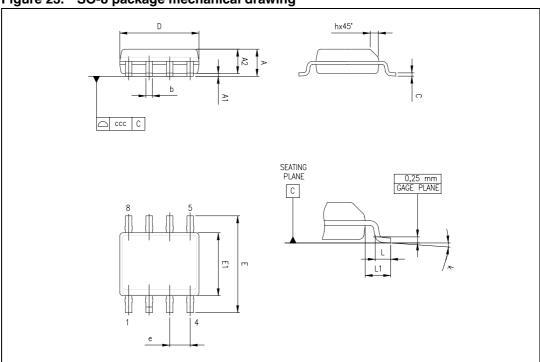


Table 5. SO-8 package mechanical data

	Dimensions					
Ref.		Millimeters			Inches	
	Min.	Тур.	Max.	Min.	Тур.	Max.
А			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
С	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
е		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0		8°	1°		8°
ccc			0.10			0.004

6 Ordering information

Table 6. Order codes

Part number	Temperature range	Package	Packing	Marking
NE555N	0°C, +70°C	DIP8	Tube	NE555N
NE555D/DT	0 0, +70 0	SO-8	Tube or tape & reel	NE555
SA555N	-40°C, +105°C	DIP8	Tube	SA555N
SA555D/DT	-40 C, +105 C	SO-8	Tube or tape & reel	SA555
SE555N	-55°C, + 125°C	DIP8	Tube	SE555N
SE555D/DT	-55 C, + 125 C	SO-8	Tube or tape & reel	SE555

NE555 - SA555 - SE555 Revision history

7 Revision history

Table 7. Document revision history

Date	Revision	Changes
01-Jun-2003	1	Initial release.
2004-2006	2-3	Internal revisions
15-Mar-2007	4	Expanded order code table. Template update.
06-Nov-2008	5	Added I _{OUT} value in <i>Table 1: Absolute maximum ratings</i> and <i>Table 2: Operating conditions</i> . Added ESD tolerance, latch-up tolerance, R _{thja} and R _{thjc} in <i>Table 1: Absolute maximum ratings</i> .

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2008 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com